Appl. No. 10/032,761
Amdt. dated August 11, 2003
Reply to Office Action of April 11, 2003

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1-5. Canceled.

6. (Currently Amended) A driver circuit integrated with a load current output circuit, comprising: a first buffer circuit having a first output terminal; a second buffer circuit having a second output terminal; and a diode bridge terminal having a pair of a third and fourth output terminals each connected to said first and said second output terminals in the form of direct current, wherein said fourth output terminal supplies a current as a driver when outputting a test waveform to a device under test (DUT), and said DUT supplies a load current to said fourth output terminal therefrom by turning the second buffer circuit OFF when judging a status of a response waveform by receiving said waveform from said DUT.

7. (Original) A driver circuit integrated with a load current output circuit according to claim 6, wherein said first and second buffer circuits are constituted of a voltage follower of a push-pull operation, provided with a first switch circuit for controlling ON/OFF of a last stage transistor of said first buffer and a second switch circuit for controlling ON/OFF of a last stage transistor of said second buffer circuit, so that when a test waveform is outputted to a device under test (DUT), said first and second switch circuits operate said first and second buffer circuit so as to supply current from output of both said first and second buffer circuits, and when a status of a response waveform is judged by receiving a response waveform from said DUT, said second switch circuit turn said second buffer circuit into a non operative state, and said first buffer circuit is controlled by said first switch circuit so as to supply a load current to said DUT by said first buffer circuit and said diode bridge.

8. (Original) A driver circuit integrated with a load current output circuit according to claim 7, wherein a constant current portion is provided and said diode bridge circuit is connected to another pair of a fifth and sixth output terminals.

9. (Original) A driver circuit integrated with a load current output circuit according to claim 6, wherein a diode opposed to said diode bridge circuit is simultaneously turned ON, and another diode opposed thereto is simultaneously turned OFF.

10. Canceled.

11. Canceled.

12. (Original) A pin electronic IC provided with said driver circuit integrated with said load current output circuit according to claim 6.

13. Canceled,

14. Canceled.

15. (Original) An IC tester provided with said driver circuit integrated with said load current output circuit according to claim 6.

16. (New) A driver circuit integrated with a load current output circuit according to claim 6, a portion of said first buffer circuit provides a portion of said second buffer circuit.

17. (New) A driver circuit integrated with a load current output circuit, comprising:

a first buffer circuit having a first output terminal coupled to a device under test (DUT);

a second buffer circuit having a second output terminal coupled to the DUT; and

a diode bridge component having third and fourth output terminals, each connected to said first and said second output terminals, the diode bridge component being configured to provide a test waveform in the form of direct current to the DUT via the fourth output terminal,

wherein the DUT supplies a load current to said fourth output terminal by turning OFF the second buffer circuit, so that a state of a response waveform received from the DUT may be determined.

18. (New) A driver circuit of claim 17, wherein the first buffer circuit includes a first transistor, the first transistor providing the first output terminal, the second buffer circuit including a second transistor, the second transistor providing the second output terminal.

19. (New) A driver circuit of claim 17, further comprising:

a first switch provided between a first power source and a control terminal of the first transistor; and

a second switch provided between a second power source and a control terminal of the second transistor.